

Features

- Advanced high cell density Trench technology
- Super Low Gate Charge
- Excellent CdV/dt effect decline
- Green Device Available

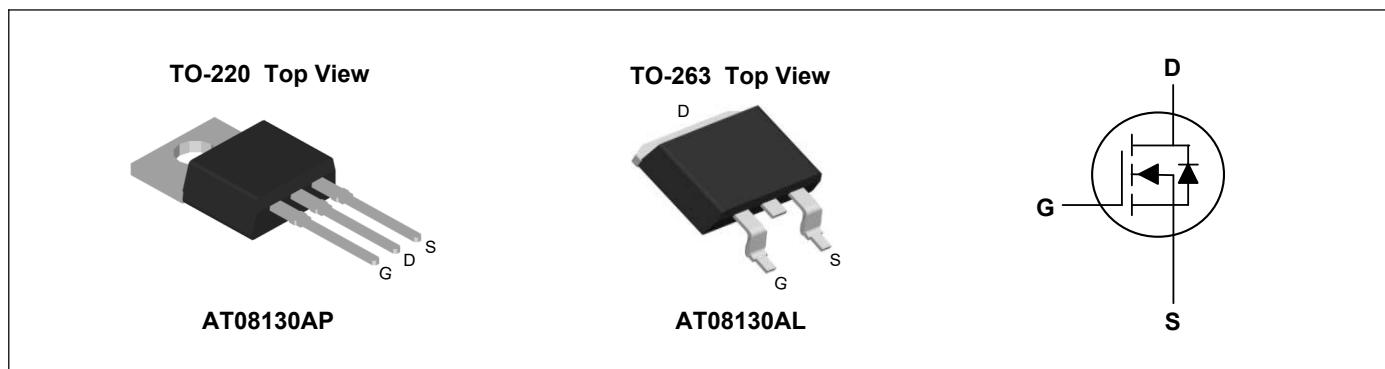
Product Summary



V_{DS}	80	V
I_D	130	A
$R_{DS(ON)}$ (at $V_{GS}=10V$)	4.5	mΩ

Applications

- High Frequency Point-of-Load Synchronous Buck Converter
- Networking DC-DC Power System
- Power Tool Application



Absolute Maximum Ratings($T_c=25^\circ C$, unless otherwise noted)

Parameter	Symbol	Rating	Units
Drain-Source Voltage	V_{DS}	80	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current	$I_D @ T_c = 25^\circ C$	130	A
Pulsed Drain Current ²	I_{DM}	390	A
Single Pulse Avalanche Energy ³	EAS	400	mJ
Total Power Dissipation ⁴	$P_D @ T_c = 25^\circ C$	192	W
Storage Temperature Range	T_{STG}	-55 to 150	°C
Operating Junction Temperature Range	T_J	-55 to 150	°C

Thermal Characteristics

Parameter	Symbol	Typ	Max	Unit
Thermal Resistance Junction-Ambient ¹	$R_{\theta JA}$	---	62	°C/W
Thermal Resistance Junction-Case ¹	$R_{\theta JC}$	---	0.65	°C/W

Electrical Characteristics ($T_J=25^\circ\text{C}$, unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{\text{GS}}=0\text{V}$, $I_D=250\mu\text{A}$	80	---	---	V
Static Drain-Source On-Resistance ²	$R_{\text{DS}(\text{ON})}$	$V_{\text{GS}}=10\text{V}$, $I_D=20\text{A}$	---	3.8	4.5	$\text{m}\Omega$
Gate Threshold Voltage	$V_{\text{GS}(\text{th})}$	$V_{\text{GS}}=V_{\text{DS}}$, $I_D=250\mu\text{A}$	2.0	---	4.0	V
Drain-Source Leakage Current	I_{DSS}	$V_{\text{DS}}=80\text{V}$, $V_{\text{GS}}=0\text{V}$, $T_J=25^\circ\text{C}$	---	---	1	uA
		$V_{\text{DS}}=80\text{V}$, $V_{\text{GS}}=0\text{V}$, $T_J=55^\circ\text{C}$	---	---	5	
Gate-Source Leakage Current	I_{GSS}	$V_{\text{GS}}=\pm 20\text{V}$, $V_{\text{DS}}=0\text{V}$	---	---	± 100	nA
Total Gate Charge	Q_g	$V_{\text{DS}}=50\text{V}$, $V_{\text{GS}}=10\text{V}$, $I_D=22\text{A}$	---	101.6	---	nC
Gate-Source Charge	Q_{gs}		---	20.6	---	
Gate-Drain Charge	Q_{gd}		---	28.7	---	
Gate plateau voltage	V_{plateau}		---	4.2	---	V
Turn-On Delay Time	$T_{\text{d(on)}}$		---	28.8	---	ns
Rise Time	T_r	$V_{\text{DS}}=50\text{V}$, $V_{\text{GS}}=10\text{V}$, $R_G=2.2\Omega$, $I_D=22\text{A}$	---	7.5	---	
Turn-Off Delay Time	$T_{\text{d(off)}}$		---	81.9	---	
Fall Time	T_f		---	20.1	---	
Input Capacitance	C_{iss}	$V_{\text{DS}}=50\text{V}$, $V_{\text{GS}}=0\text{V}$, $f=1\text{MHz}$	---	8681	---	pF
Output Capacitance	C_{oss}		---	6484	---	
Reverse Transfer Capacitance	C_{rss}		---	8.55	---	

Drain-Source Diode Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Continuous Source Current ^{1,5}	I_s	$V_{\text{GS}}=V_{\text{th}}$	---	---	130	A
Pulsed Source Current ^{2,5}	I_{SM}		---	---	390	A
Diode Forward Voltage ²	V_{SD}	$V_{\text{GS}}=0\text{V}$, $I_s=20\text{A}$, $T_J=25^\circ\text{C}$	---	---	1.3	V
Reverse Recovery Time	t_{rr}	$I_F=10\text{A}$, $\text{di}/\text{dt}=100\text{A}/\mu\text{s}$, $T_J=25^\circ\text{C}$	---	82.1	---	nS
Reverse Recovery Charge	Q_{rr}		---	248.4	---	nC
Peak Reverse Recovery Current	I_{rrm}		---	4.9	---	A

Note:

- 1.The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- 2.The data tested by pulsed , pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$
- 3.The EAS data shows Max. rating . The test condition is $V_{\text{DD}}=50\text{V}$, $V_{\text{GS}}=10\text{V}$, $L=0.5\text{mH}$, $R_G=25\Omega$
- 4.The power dissipation is limited by 150°C junction temperature
- 5.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

Typical Characteristics

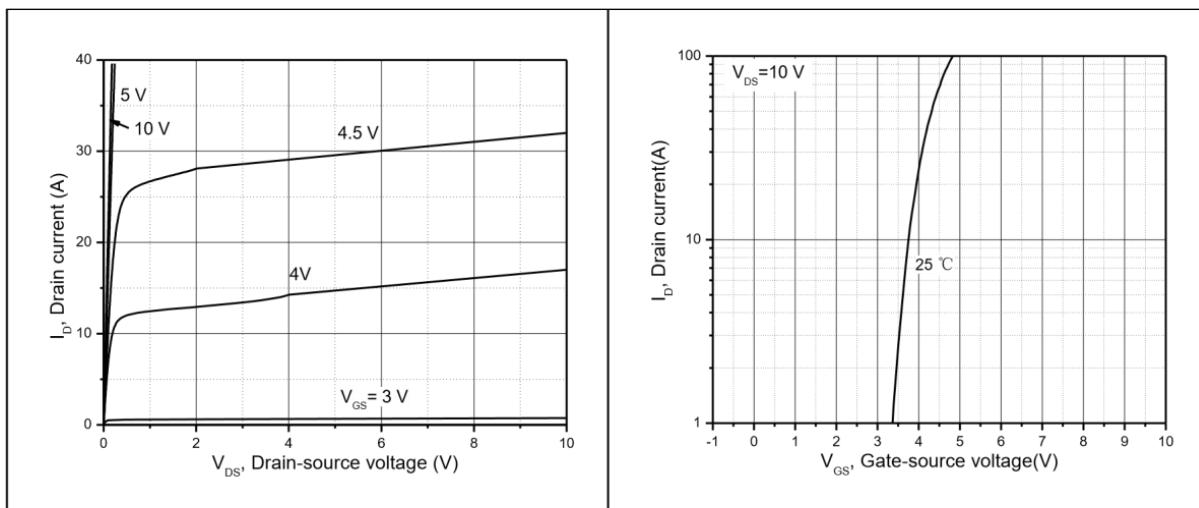


Figure 1, Typ. output characteristics

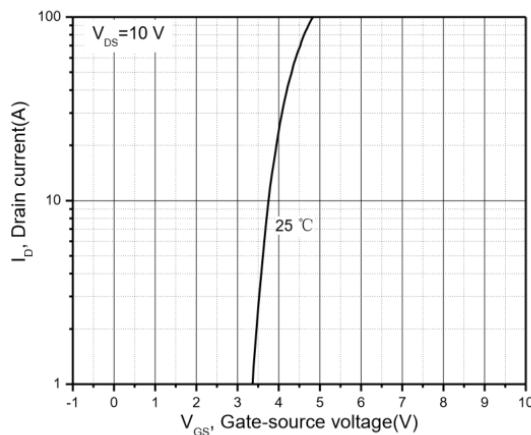


Figure 2, Typ. transfer characteristics

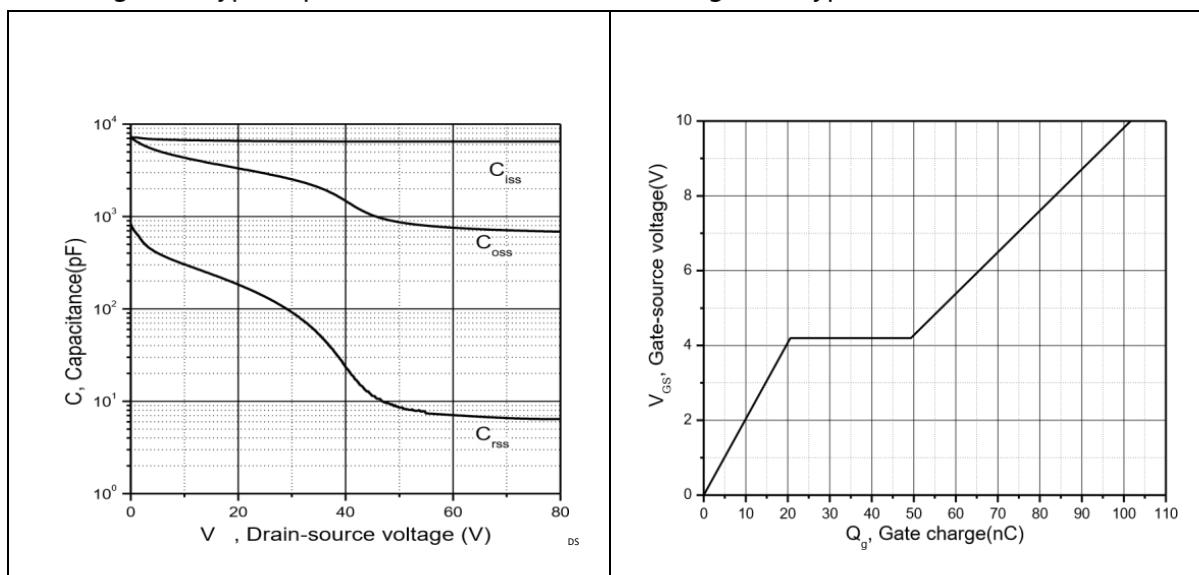


Figure 3, Typ. capacitances

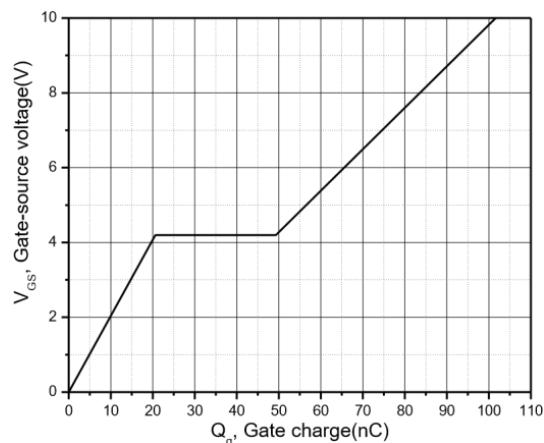


Figure 4, Typ. gate charge

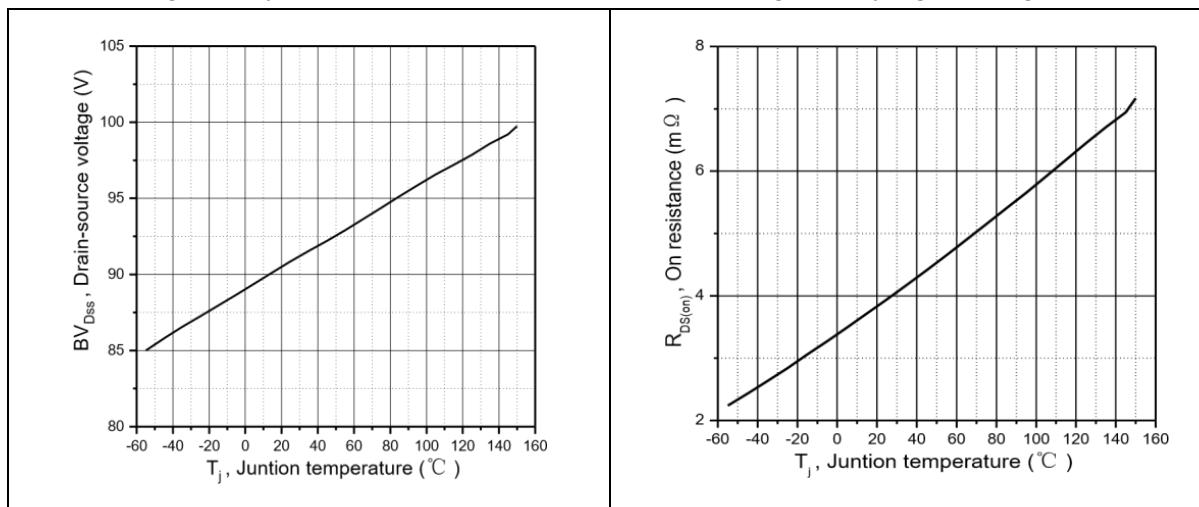


Figure 5, Drain-source breakdown voltage

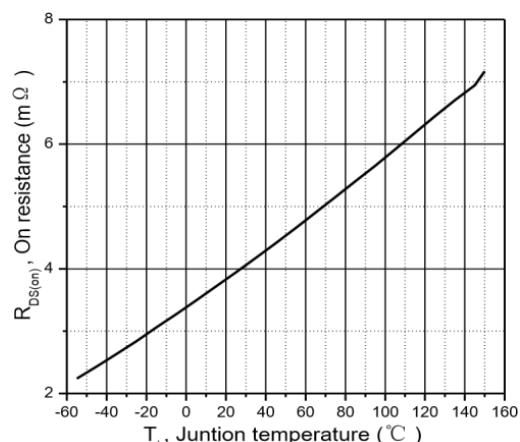


Figure 6, Drain-source on-state resistance

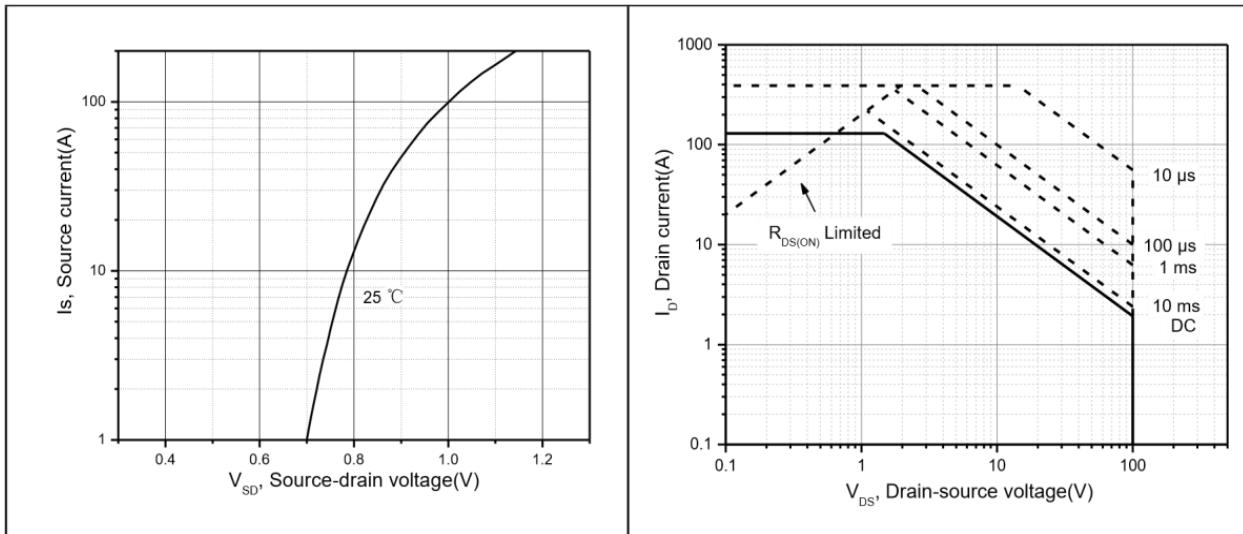


Figure 7, Forward characteristic of body diode

Figure 8, Safe operation area $T_C=25\text{ }^\circ\text{C}$

Test circuits and waveforms

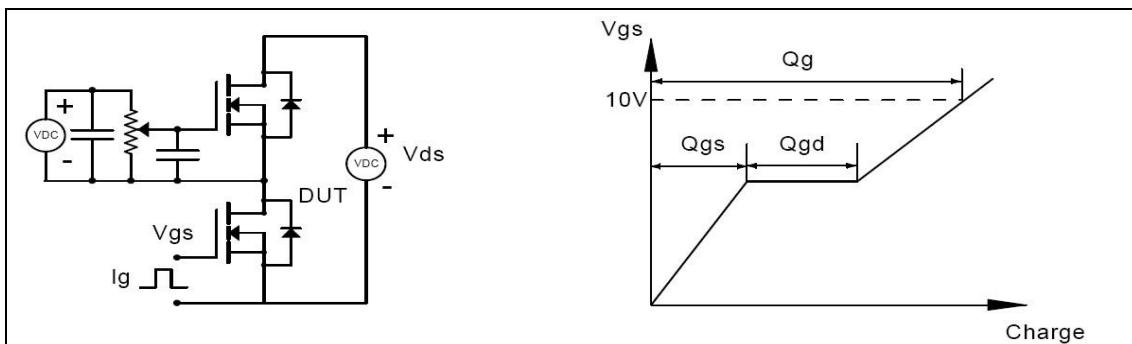


Figure 1, Gate charge test circuit & waveform

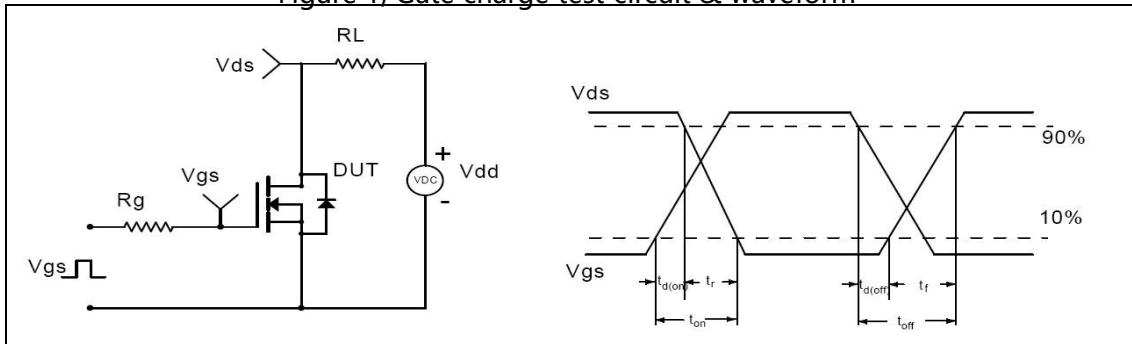


Figure 2, Switching time test circuit & waveforms

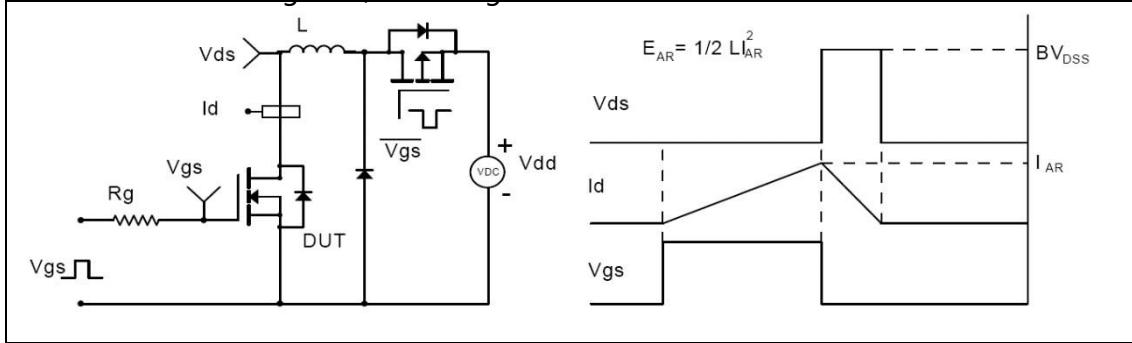


Figure 3, Unclamped inductive switching (UIS) test circuit & waveforms

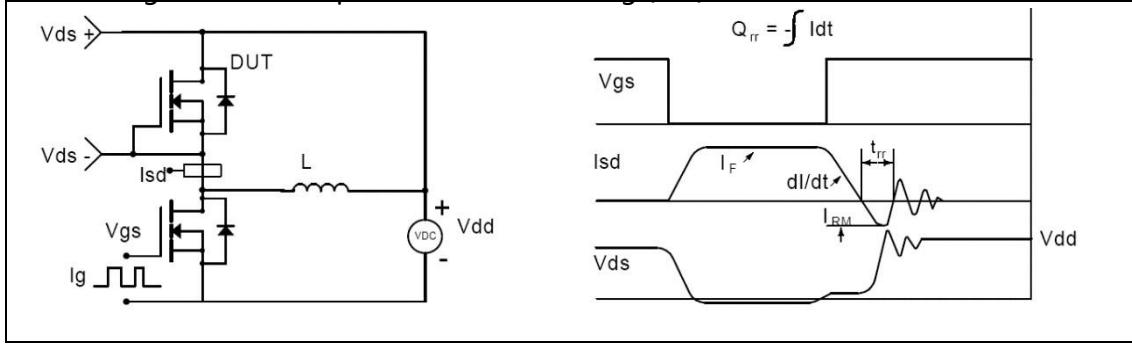
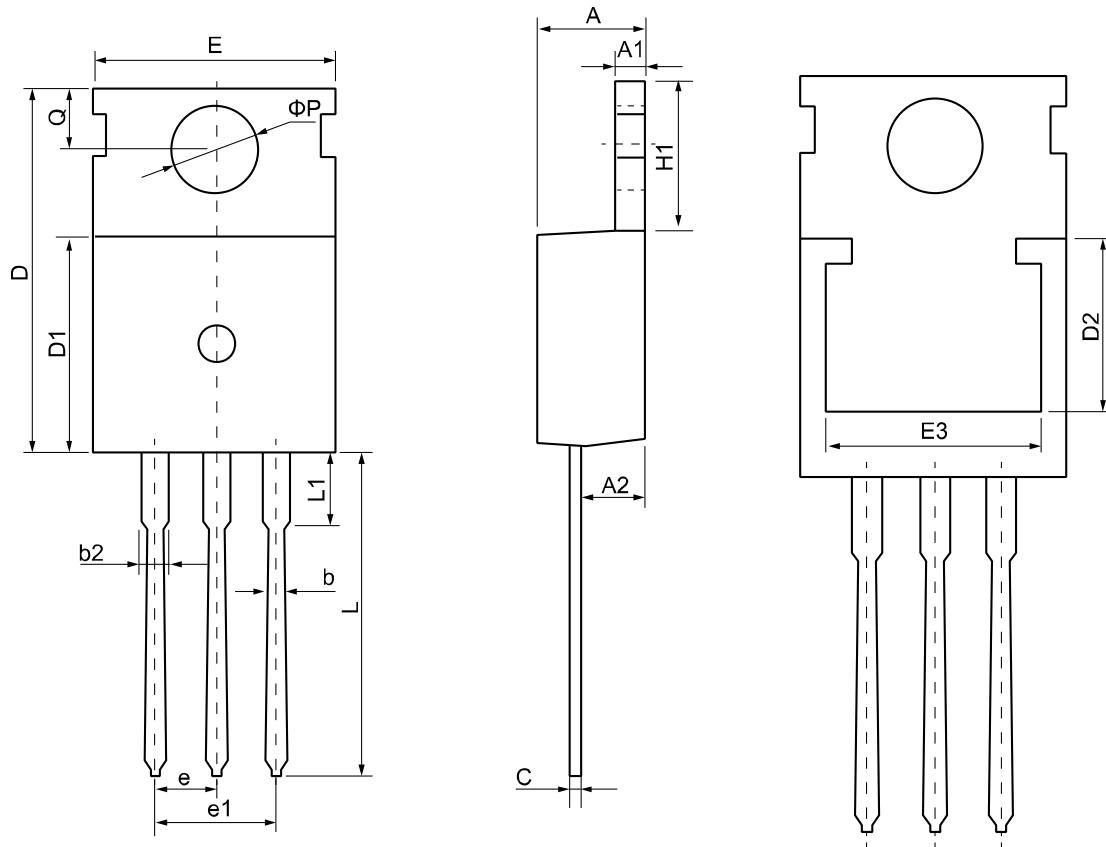


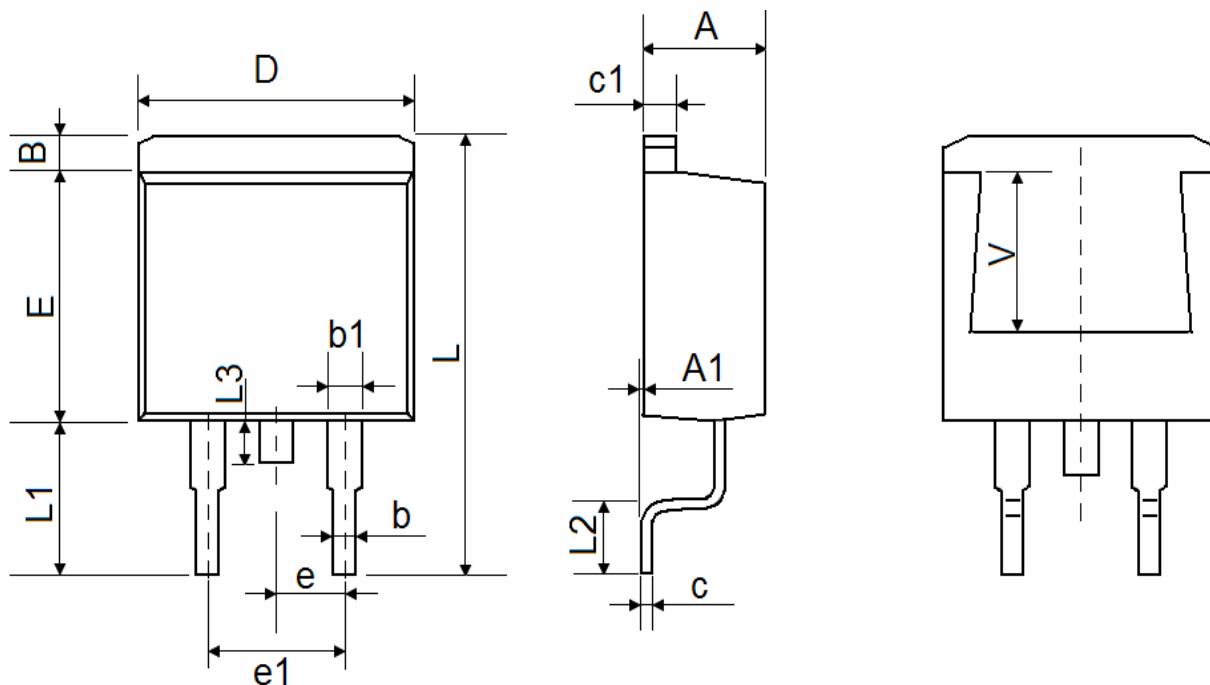
Figure 4, Diode reverse recovery test circuit & waveforms

TO-220 Package Outline Dimensions



Symbol	Dimensions (unit:mm)			Symbol	Dimensions (unit:mm)		
	Min	Typ	Max		Min	Typ	Max
A	4.30	4.55	4.75	E	9.65	10.00	10.25
A1	1.15	1.30	1.45	E3	7.00	--	--
A2	2.20	2.40	2.60	e	2.54 BSC		
b	0.70	0.80	0.95	e1	5.08 BSC		
b2	1.17	1.27	1.47	H1	6.30	6.50	6.80
c	0.40	0.50	0.65	L	12.70	13.50	14.10
D	15.30	15.60	15.90	L1	--	3.20	3.95
D1	8.90	9.10	9.35	φP	3.40	3.60	3.80
D2	5.50	--	--	Q	2.60	2.80	3.00

TO-263 Package Outline Dimensions



Symbol	Dimensions (unit:mm)			Symbol	Dimensions (unit:mm)		
	Min	Typ	Max		Min	Typ	Max
A	4.40	4.55	4.70	A1	0.00	0.07	0.15
B	1.00	1.20	1.40	b	0.65	0.80	0.95
b1	1.10	1.15	1.37	c	0.30	0.40	0.53
c1	1.10	1.25	1.37	D	9.80	10.00	10.40
E	8.50	8.80	9.20	e	2.54 REF		
e1	4.90	5.10	5.40	L	14.80	15.20	15.70
L1	5.00	5.25	5.60	L2	2.05	2.45	2.80
L3	1.20	1.50	1.80	V	5.60 REF		